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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,504	10/03/2003	Kuan-Chi Juan	WISP0033USA	2503

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,504	JUAN, KUAN-CHI	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are pending for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen U.S. Patent 5,945,817 in view of Yoon et al. U.S. Patent 6,359,459.

4. As per claim 1, Nguyen teaches a power control system used in a computer system, the power control system comprising:

a decision logic [120, 110 fig. 1; fig. 5] for detecting states of the computer system to output a decision voltage [col. 3 lines 60-65].

a voltage control [150 fig. 1] unit for outputting a set voltage according to the decision voltage outputting from the decision logic, the voltage control unit comprising:

a power supply circuit for generating an output voltage for the computer system according to the set voltage [col. 8 lines 37-57]. Nguyen further teaches, when the decision logic node PSI is at a low level indicating that the circuit generating that signal is in a low power mode, the voltage control unit in response to the signal adjusts the power supply to decrease the output voltage (or vise versa). However, Nguyen does not teach expressly the circuitry of the voltage control unit.

Yoon et al. teach a another voltage control unit [311 fig. 3] wherein the voltage control unit responsive to a control signal having a plurality of states, to generate a first reference voltage or the second voltage to power a system or a device [col. 4 lines 4-14, 22-27]. Specifically, Yoon et al. teach the voltage control unit comprising:

a first resistor [532 fig. 6]electrically connected to a voltage source;

a second resistor [533 fig. 6] electrically connected to the first resister in series connector [col. 6 lines 6-7]; and

a switch circuit [511 fig. 6] electrically connected to the first resistor in parallel connection and electrically connected to the control signal [PLVCC[1] fig. 6], wherein the switch circuit turns on or turns off according to the decision voltage outputted from the decision logic so that the voltage control unit can output the set voltage [col. 6 lines 51-65].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the voltage control unit of Nguyen with the circuitry taught by Yoon et al.

The motivation would have been to provide the system with a second power supply voltage at a magnitude that can be used to perform low voltage operation in a system without the need to reduce the external supply voltage [col. 8 lines 53-62].

Therefore, it would have been obvious to combine Nguyen with Yoon et al. to obtain the invention as specified in claim 1.

[1] The PLVCC control signal operable to control the output voltage level. Therefore, it would have been obvious to one of ordinary skill that the PLVCC control signal is part of a decision logic.

5. As per claim 2, Nguyen teaches a south bridge chip for outputting a detecting signal according to states of the computer system [col. 9 lines 34-38];

a voltage converter [fig. 5] for converting the detecting signal into a detecting voltage, the voltage converter comprising a resistor [546 fig. 5] and a capacitor [545 fig. 5]; and

a comparator [520 fig. 5] for comparing the detecting voltage with a reference voltage [VREF 515 fig. 5] to output the decision voltage.

6. As per claim 3, Nguyen teaches the decision logic comprises a current reader for outputting the decision voltage according to states of the computer system [from col. 6 line 66 to col. 7 line 16].

7. As per claim 4, Nguyen teaches the decision logic comprises a program code stored in a memory for outputting the decision voltage according to states of the computer system [col. 9 lines 16-33].

8. As per claim 5, Yoon et al. teach the switch circuit is an NMOS transistor, when the decision voltage outputted from the decision logic [obvious, see discussion in claim 1] is at a low voltage level, the switch circuit runs off; when the decision voltage outputted from the decision logic at a high voltage lever, the switch circuit conducts [col. 6 lines 51-65].

However, Yoon et al. do not teach expressly the switch circuit is an PMOS transistor.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modified the switch of Yoon et al. with a PMOS transistor because applicant has not disclosed that PMOS transistor provides an advantage, it

used to a particular purpose, or solves a stated problem. One of ordinary skill in the art, further more, would have expected applicant's invention to perform equally well with the NMOS transistor of Yoon et al. or the claimed PMOS transistor because both transistors perform the same function which is to control the level of output voltage.

Therefore, it would have been an obvious matter of design choice to modify the system of Nguyen modified by Yoon et al. to obtain he invention as specified in claim 5.

9. As per claim 6, Yoon et al. teach the switch circuit is an NMOS transistor, when the decision voltage outputted from the decision logic [obvious, see discussion in claim 1] is at a low voltage level, the switch circuit runs off; when the decision voltage outputted from the decision logic at a high voltage lever, the switch circuit conducts [col. 6 lines 51-65].

10. As per claim 7, Yoon et al. teach a third resistor electrically connected between the first resistor and the voltage source [531 fig. 6].

11. As per claim 8, Nguyen teaches the power control system used in a computers system[col. 9 line 7-15]. Therefore, it is obvious to one of ordinary skill in the art that the voltage source in Nguyen system is a battery.

12. As per claim 9, Nguyen teaches a computer system. Therefore, it is obvious to one of ordinary skill in the art that Nguyen computer system included the claimed notebook since the

special type of computer system does not alter the functions of Nguyen system modified by Yoon et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran.